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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/604,067 | 06/26/2000 | Ming-Dou Ker | TSMC2000-004 | 2697 |

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| EXAMINER | |
|---|---|
| SIRCUS, BRIAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2836 | |

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/604,067 | KER ET AL. | |
| | Examiner | Art Unit | |
| | Stephen W Jackson | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-28* is/are allowed.

6)☒ Claim(s) *1-11,13,20 and 22* is/are rejected.

7)☒ Claim(s) *12 and 14-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *26 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Maloney et al. (US 6,008,970)

a) Regarding claims 1 and 10, Maloney et al. discloses an electrostatic discharge (ESD) protection circuit (104) that is connected between a first terminal (Vcc) and a second terminal connected to ground of an Integrated Circuit (IC) (100), whereby ESD protection circuit comprises: a ESD pulse clamp means comprising a PMOS device (202) for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port connected to the gate of PMOS device (202); and an ESD pulse detection means (204) having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

b) Regarding claim 2, Maloney et al. discloses that said ESD pulse detection means contains a network comprising a resistive (215) component having a first and a second terminal, a capacitive component (209) having a first and a second terminal, and a voltage inverter(254). See col. 4 lines 53-55.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-9 and 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Ker (IEEE Transactions on Electron Devices Vol.46 No. 1) in view of Maloney et al.

Ker et al. discloses an electrostatic discharge (ESD) protection circuit (Fig. 7) that is connected between a first terminal (VSS) and a second terminal (VDD) of an Integrated Circuit (IC), whereby ESD protection circuit comprises: a ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port; and an ESD pulse detection means (R, C, Mp, Mn) having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that

triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC. Said ESD pulse clamp means comprises a CMOS device and is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said CMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said CMOS device is connected to said third port of said ESD pulse clamp means. Ker et al. does not disclose that the MOS device is a PMOS device. Maloney et al. teaches the use of PMOS devices as a voltage clamp in ESD protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ker to include PMOS device because if the known benefits of that PMOS transistors provide.

4. Claims 13 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker in view of Maloney et al. in further view of Mead (Introduction to VLSI systems)

Ker et al. in view of Maloney et al. discloses the circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises a MOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component. Ker et al. does not disclose that such the capacitive component is a PMOS device. Mead discloses the principle behind the use of MOS devices as capacitance. It is inherent that such principles apply to CMOS and PMOS devices as well. It would have been obvious to one

of ordinary skill in the art at the time the invention was made to substitute the CMOS device for a PMOS device because these two were art-recognized equivalents.

***Allowable Subject Matter***

5. Claims 14-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 21 and 23-28 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Claims 20-28 recite, inter alia, an electrostatic discharge protection circuit comprising an ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from an IC having a first port that is connected to the first terminal of the IC, a second port that is connected to the second terminal of the IC and a third port and an ESD detection means having a first input port connected to said first terminal of said IC a second input port connected to the second terminal of the IC and an output port that is connected to said third port of said ESD pulse clamp means wherein the ESD detection means has s specific configuration.

Ker (IEEE transactions on electron devices vol. 46 no. 1) discloses the specific configuration but does not disclose a PMOS transistor.

Lien (US 5,086,365) discloses an ESD protection device with a PMOS transistor but does not disclose the specific configuration.

Maloney et al discloses an electrostatic discharge (ESD) protection circuit with a PMOS voltage clamp and an ESD detection circuit, but the ESD detection circuit does not have the specific configuration.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such a limitation.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W Jackson whose telephone number is 571-272-2051. The examiner can normally be reached on 6:30am-3:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWJackson

March 24, 2004

Stephen W. Jackson 3-24-04

STEPHEN W. JACKSON
PRIMARY EXAMINER